Outline

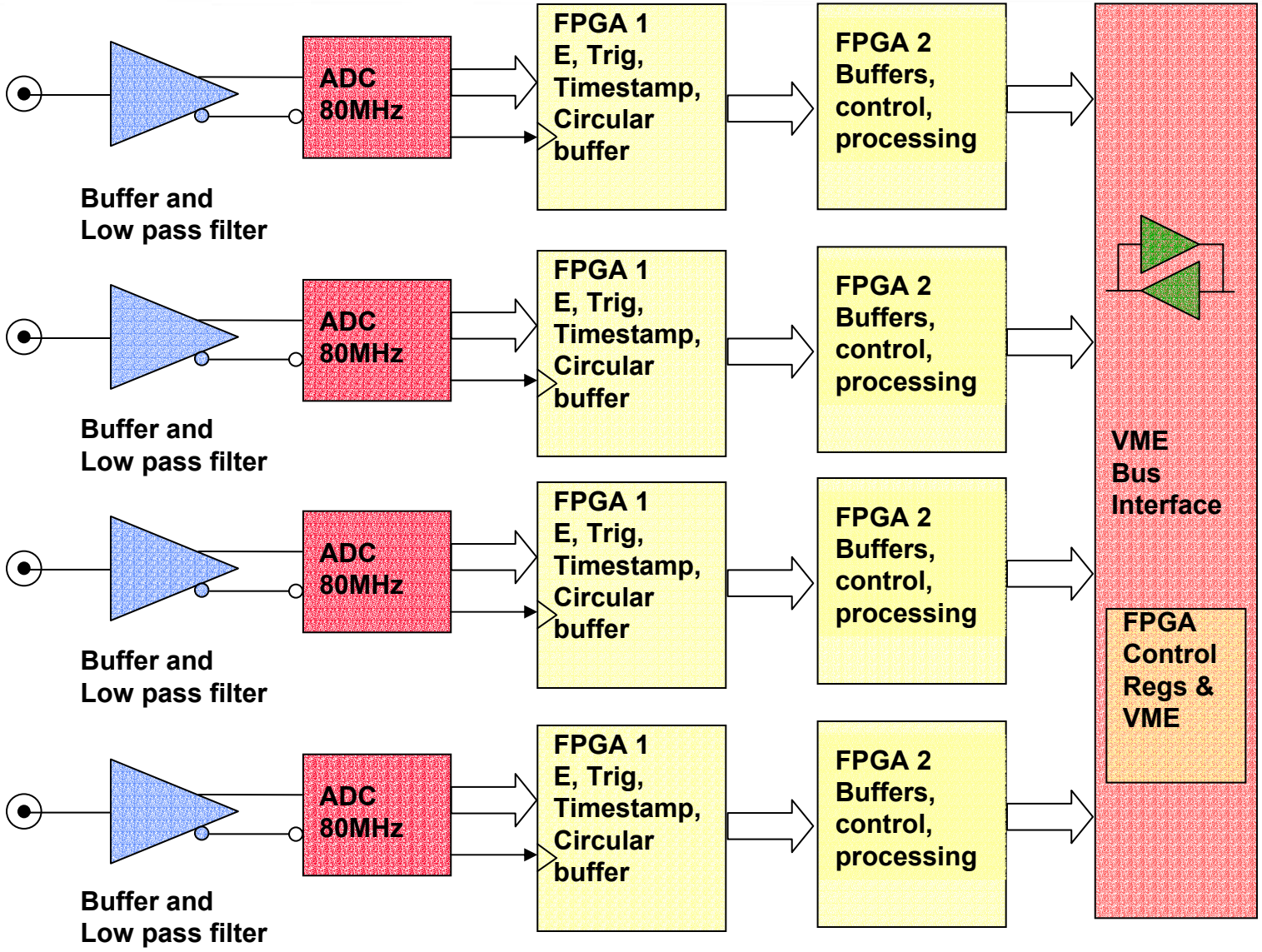
- Why we built the GRT4
- What's in the GRT4
- GRT4 system used in Cologne (Feb 2003)
- MWD implementation (Martin Lauer)
- Advantages and disadvantages of the GRT4
- Outlook- what next?

Why did we make the GRT4?

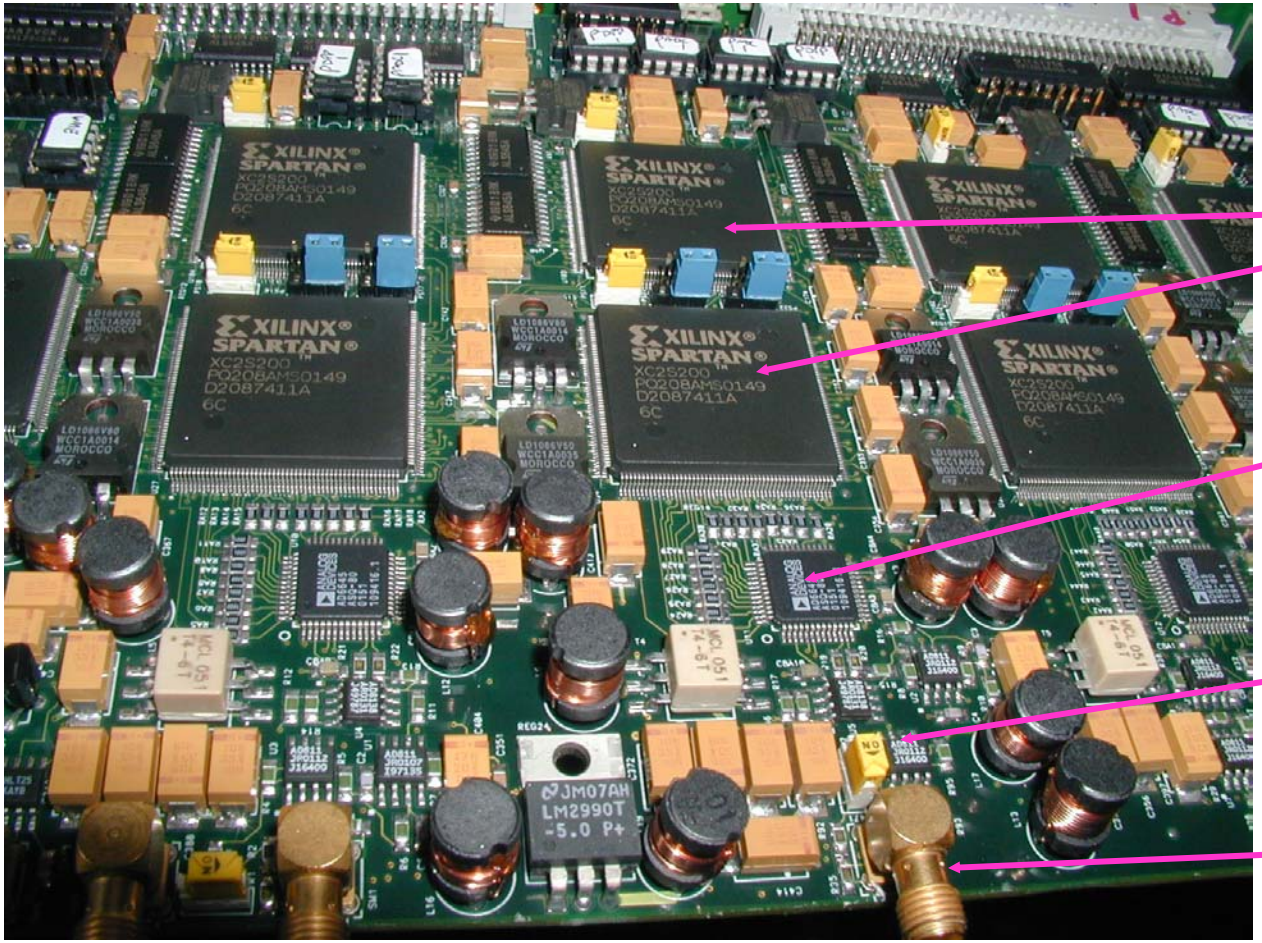
- The motivation came from Gamma Ray Tracking:
  - To characterise segmented Ge detectors
  - To collect high resolution trace data
  - To investigate and develop hardware algorithms
- **Ideal** for scanning table systems (e.g.Liverpool University)
- **Not** intended for high rate multi-channel systems
- Also in use for Medical Imaging project with Ge pixel detectors at UCL.

  (Gary Royle et al *"The Development of a Pixellated Germanium Compton Camera for Nuclear Medicine"* presented at 2003 IEEE-MIC)

GRT4 Block Diagram



GRT4 Picture



Two FPGAs
Per input (400k gates)

14 bit 80MHz
AD6645 ADCs

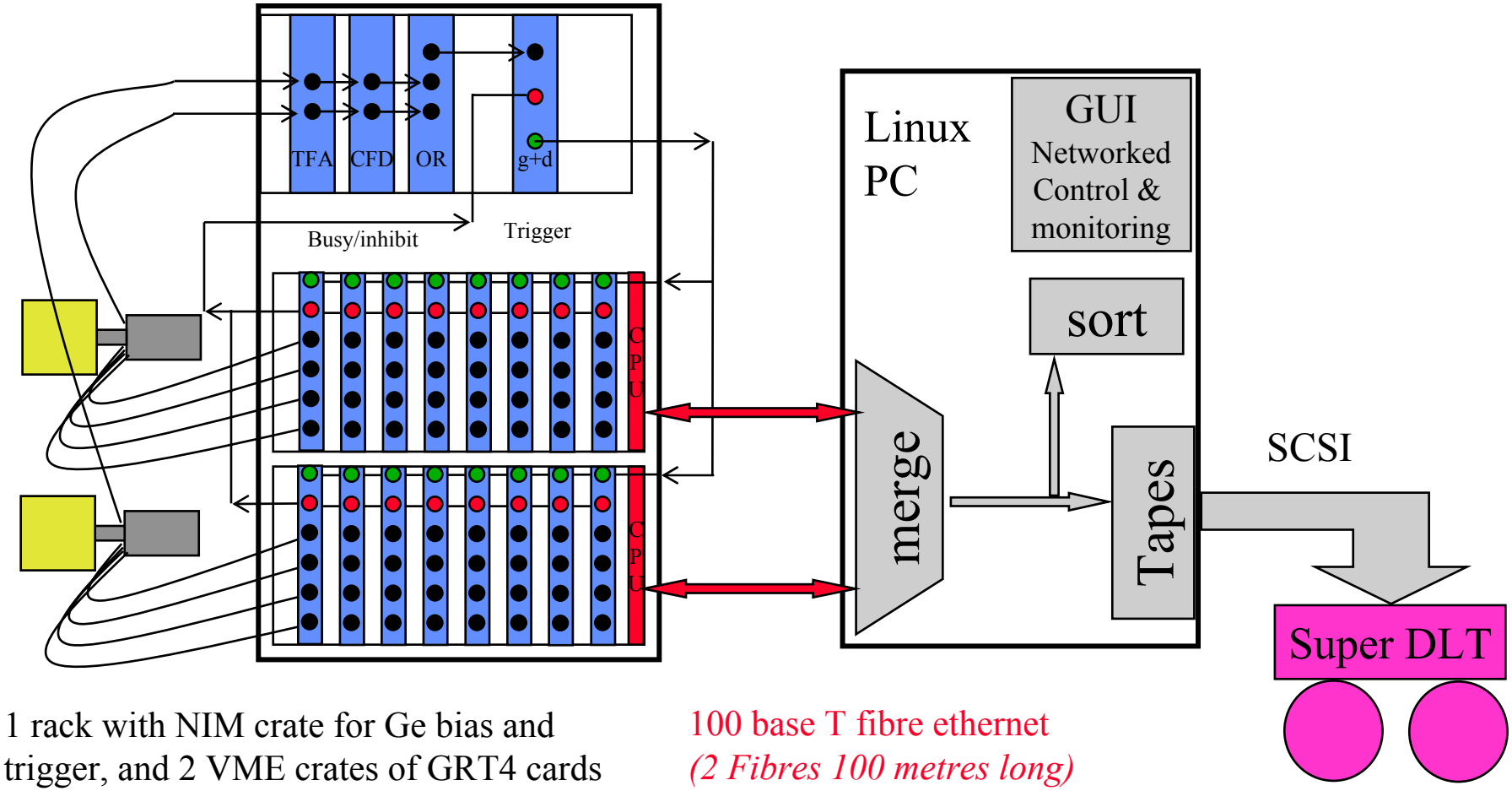
Switchable differentiation

SMA 50ohm
Inputs (4)

GRT4 outline specification

- 4 inputs: 0-550mV into 50ohms Gain is x2
- Between input and ADC are a 40MHz bandwidth low pass filter and optional differentiator (Full scale = 15mV/ns slew.)
- ADCs are 14 bits, 80 MHz
- Trigger Input (Fast NIM)
- Busy Out (can be changed under s/w control to be used as Trigger output (Fast NIM))
- Gate In (can be used either as trigger gate or else to synchronise timestamps) (Fast NIM)

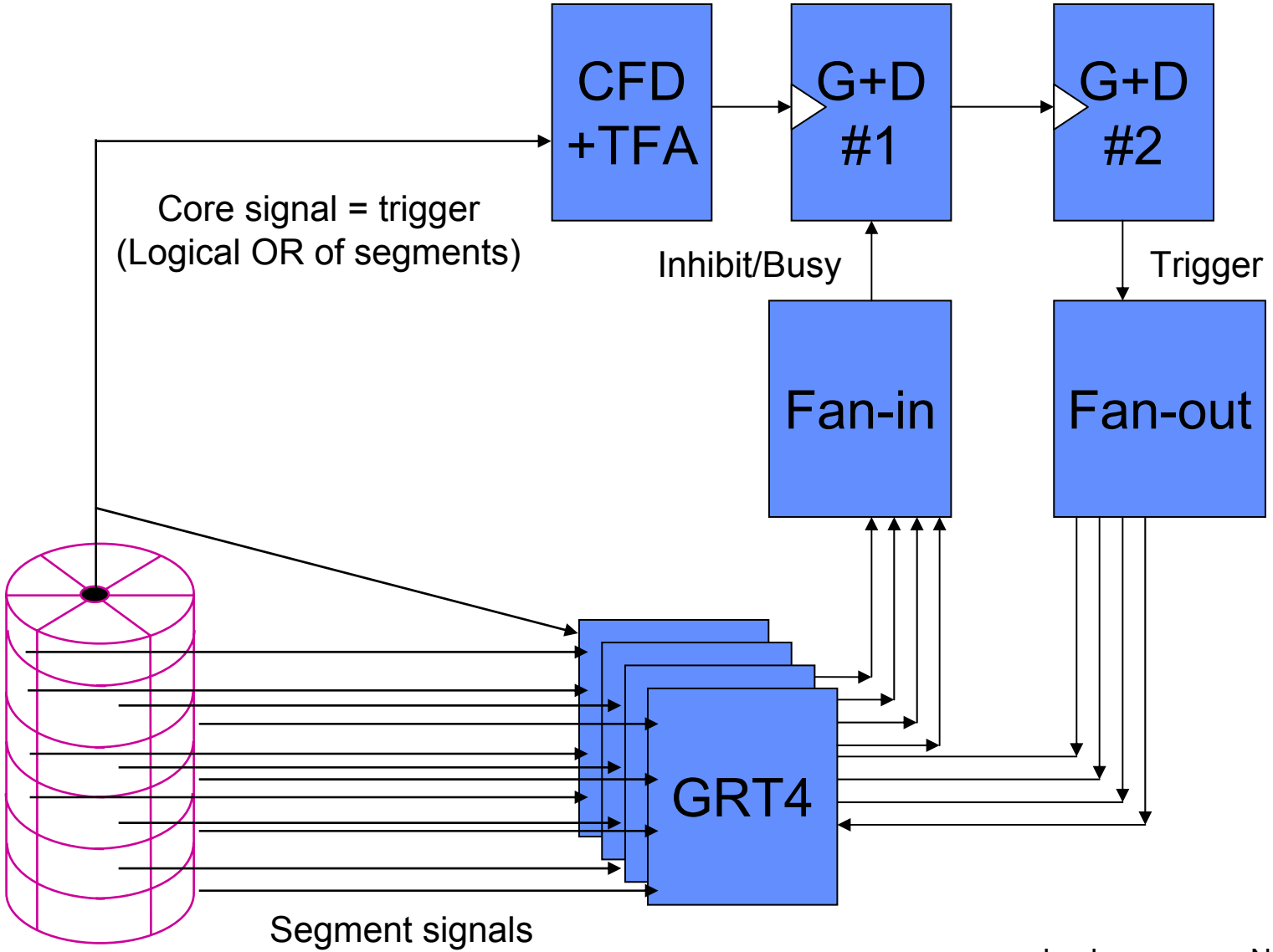
DAQ for Cologne Test Run



1 rack with NIM crate for Ge bias and trigger, and 2 VME crates of GRT4 cards

100 base T fibre ethernet
(2 Fibres 100 metres long)

Flow control & trigger for seg coax Ge



MWD Implementation Highlights

GRT4 features (per channel):

- 2 XILINX Spartan2 XC2S200: 1 x preprocessing & 1 x pulse processing
- AD6645 14 bit/80 Mhz flash ADC
- more information: http://nnsa.dl.ac.uk/GRT/grt4_brochure.pdf

MWD features:

a) shaping:

- Spartan2 DLL: CLK DIVIDER [1.5, 16] → CLK and DATA decimation
- Spartan2 Block Memory: 14 dual ported memory units each 16 x 256
- possible shaping times: CLKDIV 4 → 50 ns ... 12.8 µs
  CLKDIV 16 → 200 ns ... 51.2 µs

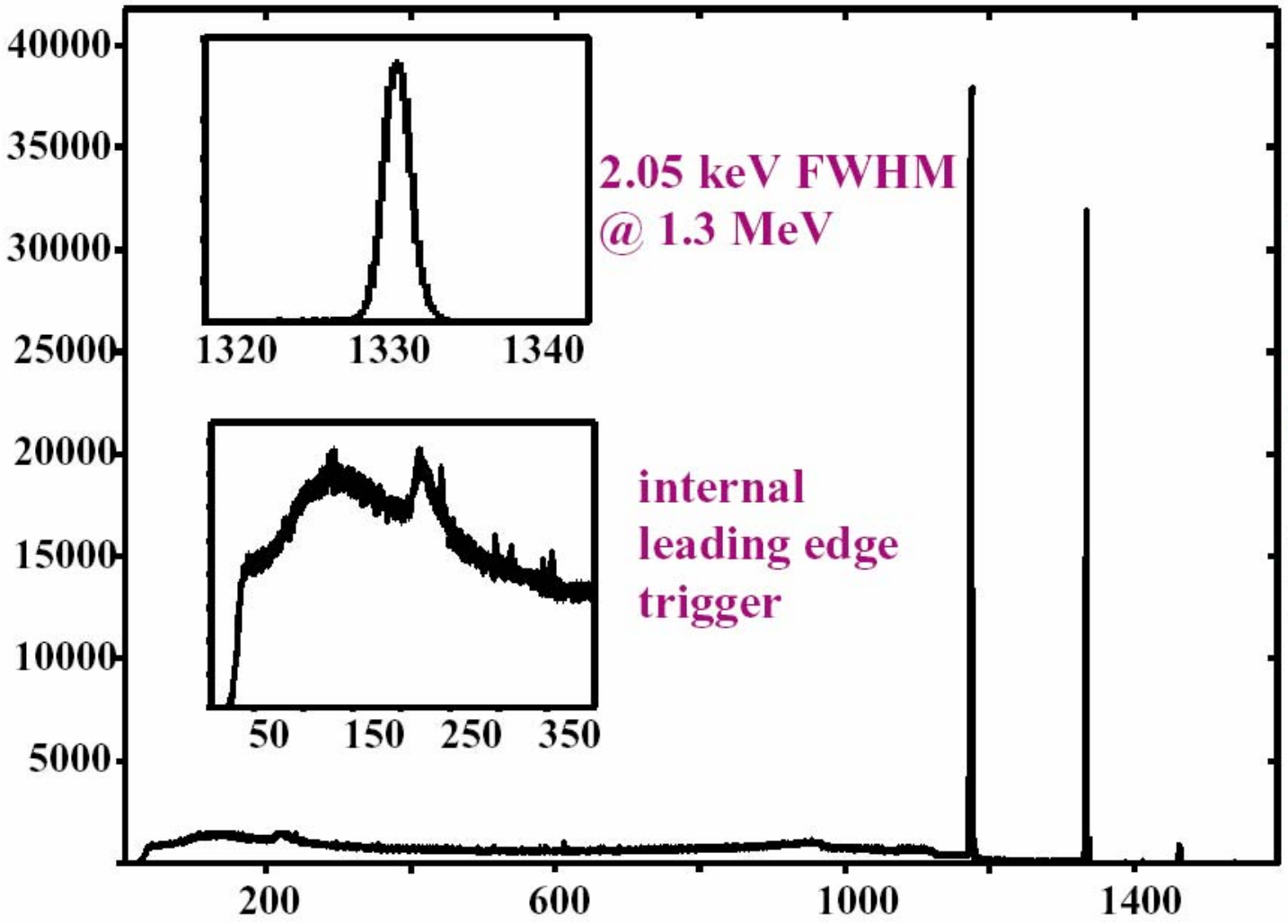
b) deconvolution:

- 24 x 24 fixed point multiplier, LUT based, not pipelined

c) Baseline Average: recursive filter or moving average filter

d) 100 MHz compliant !

GRT4 + MWD: First Results



- ^{60}Co source
- HPGe Detector: Ortec 33 % eff.

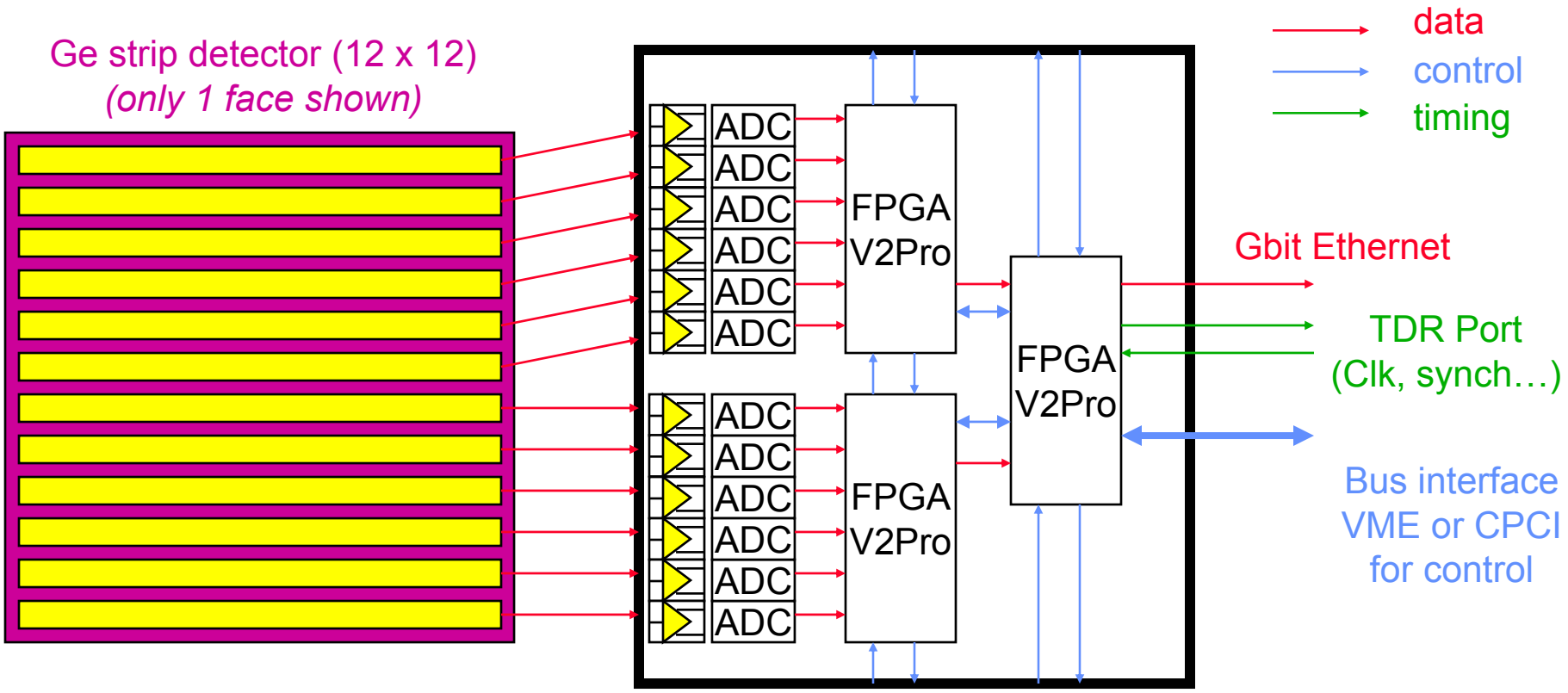
1.23keV FWHM for the 122keV peak in the ^{152}Eu spectrum.

Count rate 800Hz in both cases

Advantages & disadvantages of GRT4

- **Positive**
  - Fast enough
  - Resolution good (
  - Processing power ok
  - Cheap (not commercial)
  - Optional hardware differentiation
  - Exists and works.
  - 4ch per single width VME
- **Negative**
  - Uses 16 bit transfers over shared VME bus *(max 3.8MB/sec/crate e.g. 4kHz for 64ch, 8 words/ch)*
  - No communication with neighbour cards for position
  - No common clock
  - 4 channels per single width VME

What next?


Ge strip detector (12 x 12)
(only 1 face shown)
ADC
ADC
ADC
ADC
ADC
ADC
ADC
ADC
ADC
ADC
ADC
ADC
FPGA
V2Pro
FPGA
V2Pro
FPGA
V2Pro
data
control
timing
Gbit Ethernet
TDR Port
(Clk, synch…)
Bus interface
VME or CPCI
for control

SMARTPET electronics

- Analogue input buffer stage with gain adjust, level shift, Nyquist filter, differential output
- ADC: 14 bits 100MHz (AD6645 or ADS5500 or …?)
- FPGA: Virtex 2 Pro (e.g. 30k logic cells XC2VP30-5FG676C)
- Links to send hit patterns, trace or computed data to:
  - adjacent strips (same card or another card)
  - opposite face
  - opposite detector (PET)
- Gbit Ethernet output port: up to 100Mbytes/sec over Cat 5 twisted pair (= up to 150bytes/ADC @50kHz)
- TDR Port for synchronised counter system using Metronome:
  - Clock (100MHz or less) (in)
  - Synch pulse (in)
  - Reset (in)
  - Error (out)